Successful Application of Open Architecture Development

DoD Embedded Systems

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Open Architecture Goals[1] For SOSA, CMOSS, and HOST

- **Enable cost savings/cost avoidance through reuse**
- **Facilitate technology refresh**
  - Delivery of new capabilities or replacement technology without changing all components in the entire system

- **Improve interoperability**
  - Independently exchange software and hardware modules
- **Faster incorporation of innovation**
  - Operational flexibility to rapidly configure and reconfigure available assets to meet rapidly changing operational requirements
- **Enhance competition**
  - Open architecture with severable modules, allowing components to be openly competed

1. https://www.acq.osd.mil/se/initiatives/init_mosa.html

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Who's Who (or acronym definition)

- **HOST**
  - Hardware Open Systems Technologies standard
  - Initiated by US Navy's Naval Air Systems Command (NAVAIR) Patuxent River MD ~2014
- **CMOSS**
  - Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR) / Electronic Warfare (EW) Modular Open Suite of Standards
  - Initiated by US Army's Communications-Electronics Research, Development and Engineering Center (CERDEC) at Aberdeen Proving Grounds MD ~2013
- **SOSA**
  - Sensor Open System Architecture Standard
  - Initiated by US Air Force's Life Cycle Management Center (AFLCMC) at Wright-Patterson AFB, Ohio as an Open Group committee
    - Incubated in the Future Airborne Computing Environment (FACE) Consortium in ~2015
    - Stood up as consortium November 2017

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What is HOST?

- **A specification methodology for state-of-the-art embedded systems development and acquisition**
  - Extensible beyond its current avionic and ground vehicle focus
- **A compilation of established industry standards**
  - Mainly defines module level requirements
  - Additionally includes requirements applicable to chassis
- **Started with an OpenVPX Tier 2 standard**
  - Adds specificity to VITA's OpenVPX 65 standard (e.g. limits the "shopping list" of options)
  - Flexibility to add new Tier 2 standards for other technologies
- **Focused on establishing interoperability and interchangeability at the module level**

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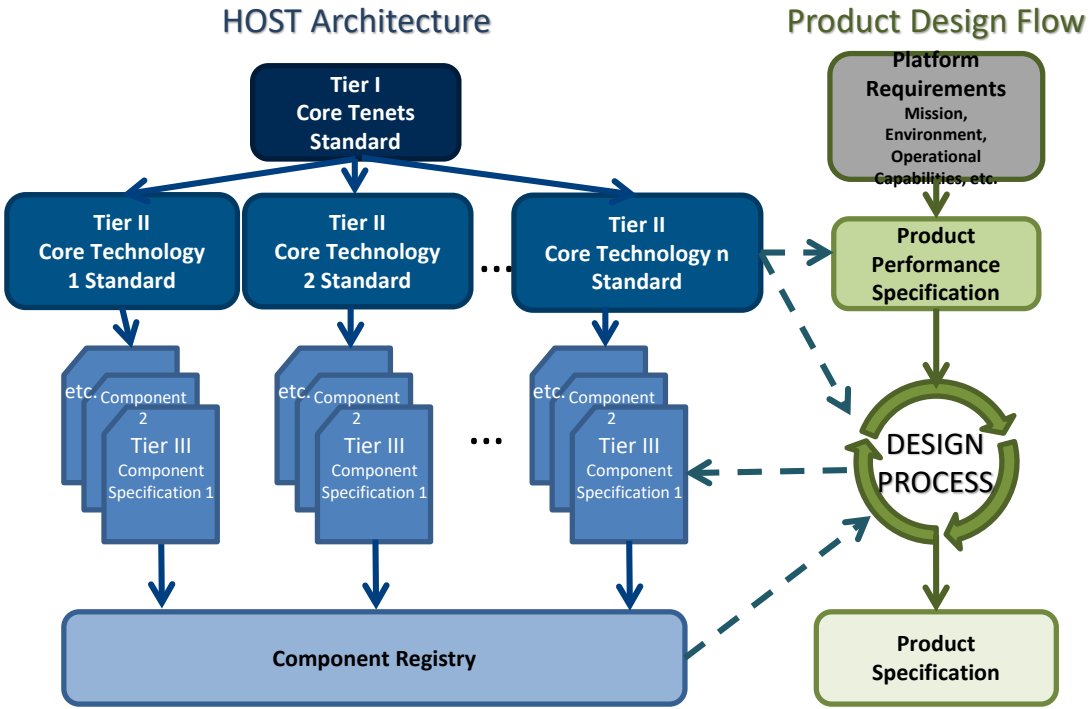
Applying HOST Standards



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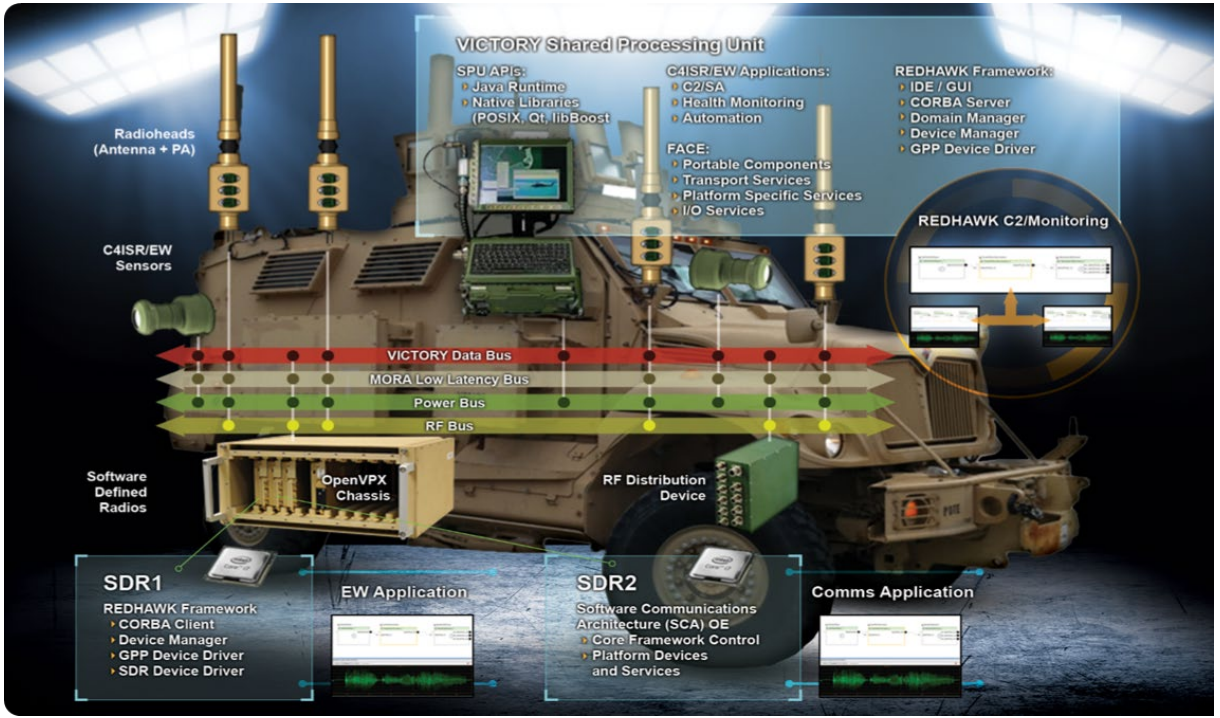
CMOSS Vision



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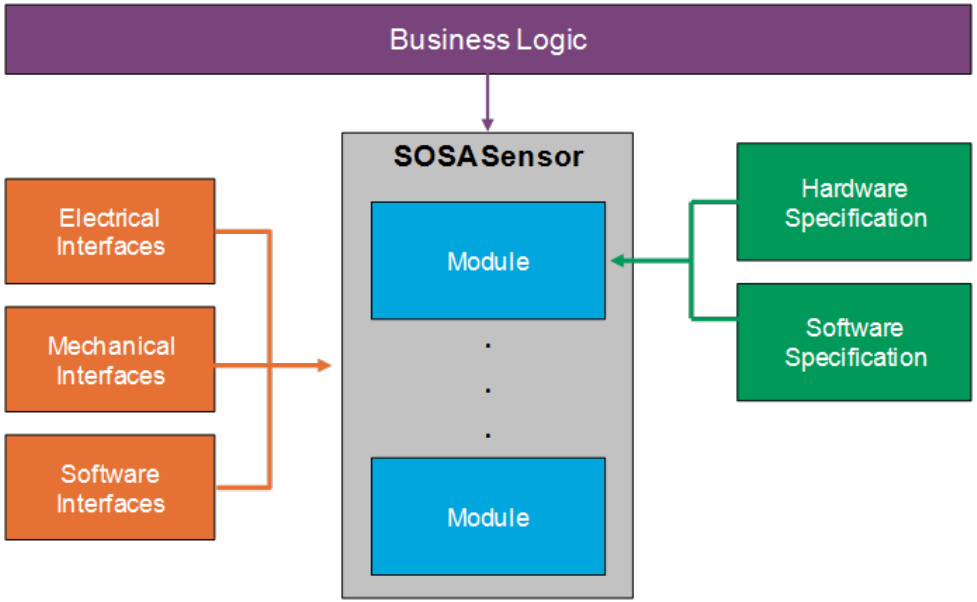
Facets that Comprise a SOSA Module



- **SOSA specifications are based on convergence of domains of knowledge for: business logic (market and government-driven forces), and technical (software, hardware, and electrical/mechanical interfaces).**

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HOST's Acquisition Success Stories

- **Joint Strike Fighter (JSF) F-35 Technology Refresh 3**[1]
  - Integrated Core Processor (ICP)
  - Panoramic Cockpit Display Electronic Unit (PCDEU)

- **Mission Computer Alternative**
  - A family of mission computers under development for legacy aircraft

- **Future Vertical Lift**

[1] "Lockheed Martin Selects Harris Corporation to Deliver F-35's Next Generation Computer Processor," September 27, 2018, https://www.f35.com/news/detail/lockheed-martin-selects-harris-corporation-to-deliver-f-35s-next-generation

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NEWS

Lockheed Martin Selects Harris Corporation to Deliver F-35's Next Generation Computer Processor

September 27, 2018

FORT WORTH, Texas, Sept. 27, 2018 – Lockheed Martin (NYSE: LMT) has selected Harris Corporation (NYSE: HRS) to develop and deliver the next generation Integrated Core Processor (ICP) for the F-35 (http://www.f35.com/) fighter jet. The Lockheed Martin-led competition within the F-35 supply chain will significantly reduce cost and enhance capability.

The F-35's ICP acts as the brains of the F-35, processing data for the aircraft's communications, sensors, electronic warfare, guidance and control, cockpit and helmet displays.

"We are aggressively pursuing cost reduction across the F-35 enterprise and, after conducting a thorough review and robust competition, we're confident the next generation Integrated Core Processor will reduce costs and deliver transformational capabilities for the warfighter," said Greg Ulmer, Lockheed Martin vice president and general manager of the F-35 program. "The next generation Integrated Core Processor for the F-35 will have positive benefits for all customers in terms of life cycle cost, capability, reliability and more."

Reduce Costs, Increased Performance

The Harris-built ICP will be integrated into F-35 aircraft starting with Lot 15 aircraft, expected to begin deliveries in 2023. The next generation ICP system is targeted to generate the following results compared to the current system:

- 75 percent reduction in unit cost
- 25 times increase in computing power to support planned capability enhancements
- Greater software stability, higher reliability, and increased diagnostics resulting in lower sustainment costs
- An Open System Architecture to enable the flexibility to add, upgrade and update future capabilities

"The new F-35 ICP will pave the way for system scalability well into the future," said Ed Zoiss, president, Harris Electronic Systems. "Open systems are the future of avionics and Harris has invested substantial R&D to deliver more affordable and higher performance solutions than would have been possible using proprietary technology."

[1] "Lockheed Martin Selects Harris Corporation to Deliver F-35's Next Generation Computer Processor," September 27, 2018, https://www.f35.com/news/detail/lockheed-martin-selects-harris-corporation-to-deliver-f-35s-next-generation

CMOSS's Acquisition Success Stories

- **Multi-Function Electronic Warfare Air Large (MFEW-AL)**
  - Offensive Electronic Attack / Electronic Warfare Support System to be mounted on a Class IV Unmanned Aircraft System (UAS)
  - MFEW-AL Capabilities Description Document (CDD) was validated by the Army on 8 December 2017
  - Prototype project awarded using Consortium for Command, Control, and Communications in Cyberspace (C5) Other Transaction Authority (OTA)

- **PEO C3T Rapid Innovation Fund (RIF) Requirement – Hardware and Software Convergence**
  - Develop and demonstrate a reliable and secure Radio Frequency (RF) communications capability on chassis card modules which supports converged platform architecture
  - Comply with the Software Communications Architecture (SCA), support the Joint Tactical Radio System (JTRS) compliant waveforms, and implement the Soldier Radio Waveform (SRW)
  - Awarded using the FY 2017 RIF Broad Agency Announcement (BAA)
- **Joint Battle Command – Platform (JBC-P)**

JBC-P Program Overview

Program Overview

Mission Statement:

To build on proven successes integrating warfighting capabilities providing a robust, secure, simple, and sustainable Mission Command system. This system provides real-time, relevant C2 information allowing leaders to gain tactical situational awareness and understanding to operate and win in a complex world.

Characteristics / Description:

- **The JBCP program consists of three core capabilities:**

1. **Hardware:**
   Mounted Family of Computer Systems (MFOCS), KGV-72, BFT & GPS Transceivers
2. **Software:**
   Joint Battle Command Platform (JBCP)
3. **Network:**
   Blue Force Tracking (BFT1 and BFT2), Network Operations Center

Soldier sees...

BFT-2 Ground Satellite Transceiver

KGV-72 Programmable In-line Encryption Device

FBCB2 Legacy Hardware (JV-5) ~ LEGACY ~

JBC-P Software Interoperable with Legacy HW and designed for the Modernized HW

Modernized JBC-P Hardware Mounted Family of Computing Hardware (MFoCS) ~ NOW FIELDING ~

PEO C3T PROGRAM EXECUTIVE OFFICE COMMAND CONTROL COMMUNICATIONS-TACTICAL

Dominate Through Seamless Mission Command

U.S. ARMY

26 November 2018

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JBC-P Program Overview

Basis of Issue: 120K Platforms

Notable Platforms: US Army

Notable Platforms: USMC

Notable Platforms: Navy & Air Force

PEO C3T — PROGRAM EXECUTIVE OFFICE COMMAND CONTROL COMMUNICATIONS-TACTICAL

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JBC-P Program Overview

Technology Transition to Product Office

- NOV - DEC 2018:
  - a) Explore Existing and Emerging CMOSS Compliant Hardware
    - Open VPX Backplane and Chassis
    - Card Configurations and Capabilities
  - b) Brief FY21-25 JBCP Program Objective Memorandum (POM) Defining Funding for Next-Generation HW Requirements

- JAN - MAR 2019:
  - a) Establish CERDEC FSA Support to JBCP Product Office
  - b) Dedicate CERDEC HMMWV and Stryker Platforms at Ft. Dix, NJ to Serve as Vehicle Integration Test Platforms

- APR - JUN 2019:
  - a) Port JBCP SW into Card Format
  - b) JBCP Product Office Hosts 1st in Recurring Series of Industry *HW/SW Convergence* Experiment Exercises to Demonstrate Technology Maturity and CMOSS Conformance

- JUL - SEP 2019:
  - a) Scope Requirements for 1st Generation HW Increment
  - b) Release RFI(s) to Industry
- OCT - DEC 2019:
  - a) 2nd *HW/SW Convergence* Experiment Exercise
  - b) Release RFP to Industry for 1st Gen HW Increment

1st Generation HW Development

Schedule and Events Tentative and Subject to Change

PEO C3T — PROGRAM EXECUTIVE OFFICE COMMAND CONTROL COMMUNICATIONS-TACTICAL

Dominate Through Seamless Mission Command

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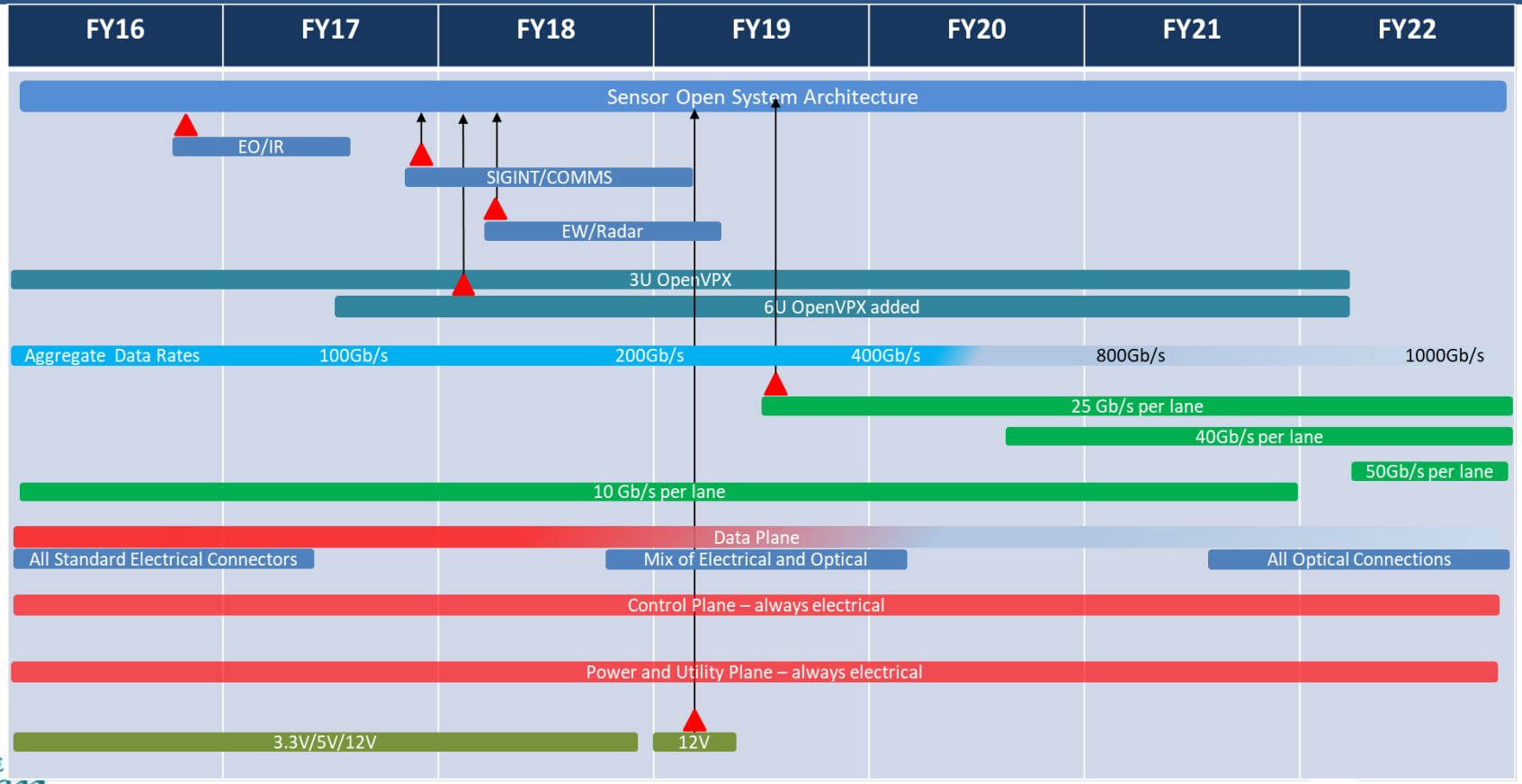
CMOSS's Foreign Adoption

- **United Kingdom (UK) Ministry of Defence (MoD)**
  - The UK MoD is considering the use of the MORA and OpenVPX elements of CMOSS as part of a Future Force Protection procurement programme
  - Currently in its concepts and assessments phase, the work continues to identify and understand opportunities to exploit relevant open standards in development (both nationally and internationally) in order to deliver the next generation of cutting-edge capabilities
- **Canadian Department of National Defence (DND)**
  - Defence Research and Development Canada (DRDC) is leveraging MORA as part of an RF Conditioning and Distribution (RCD) prototype

SOSA Hardware Working Group Roadmap



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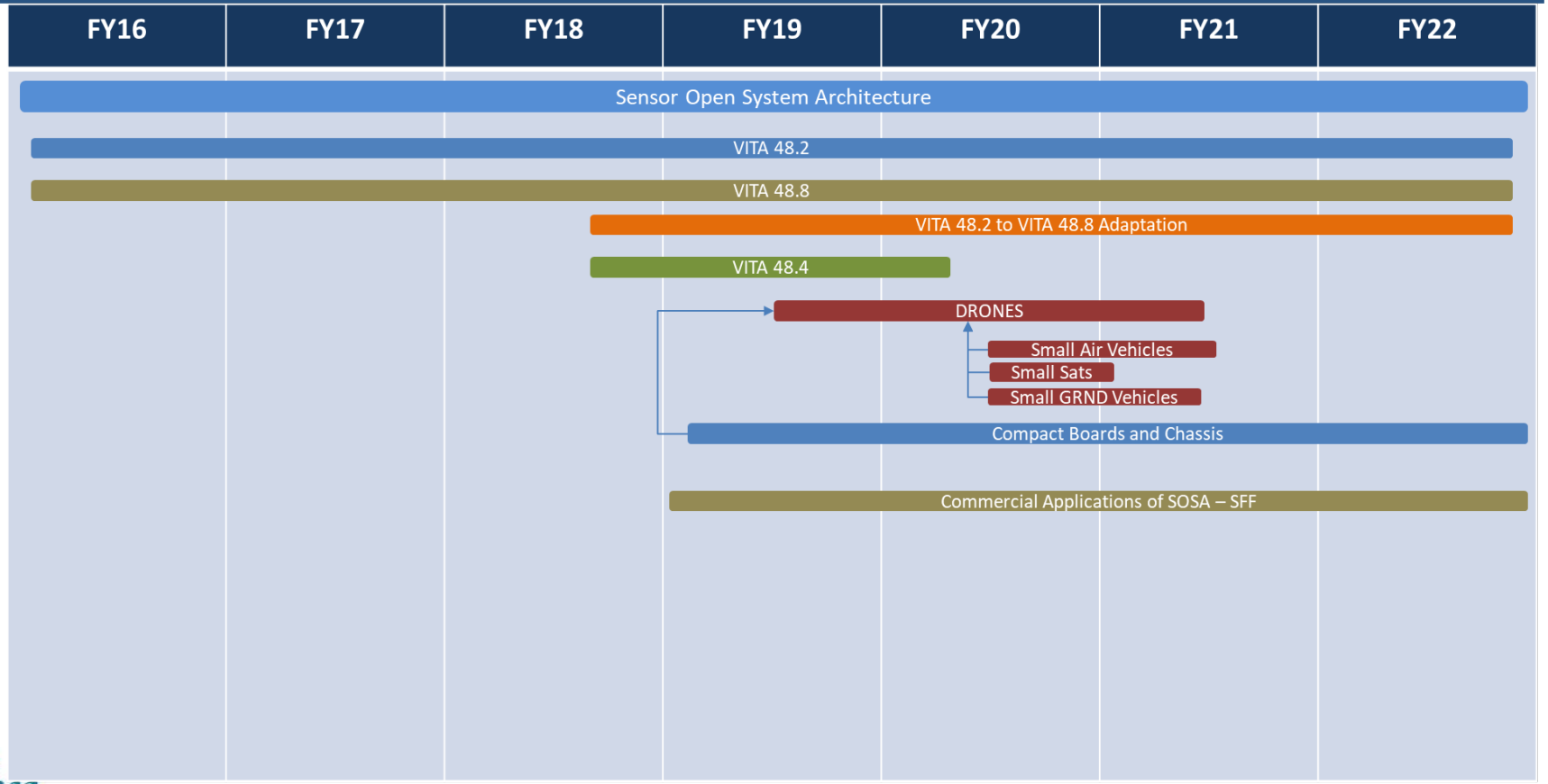
SOSA Hardware Working Group Roadmap Cont.



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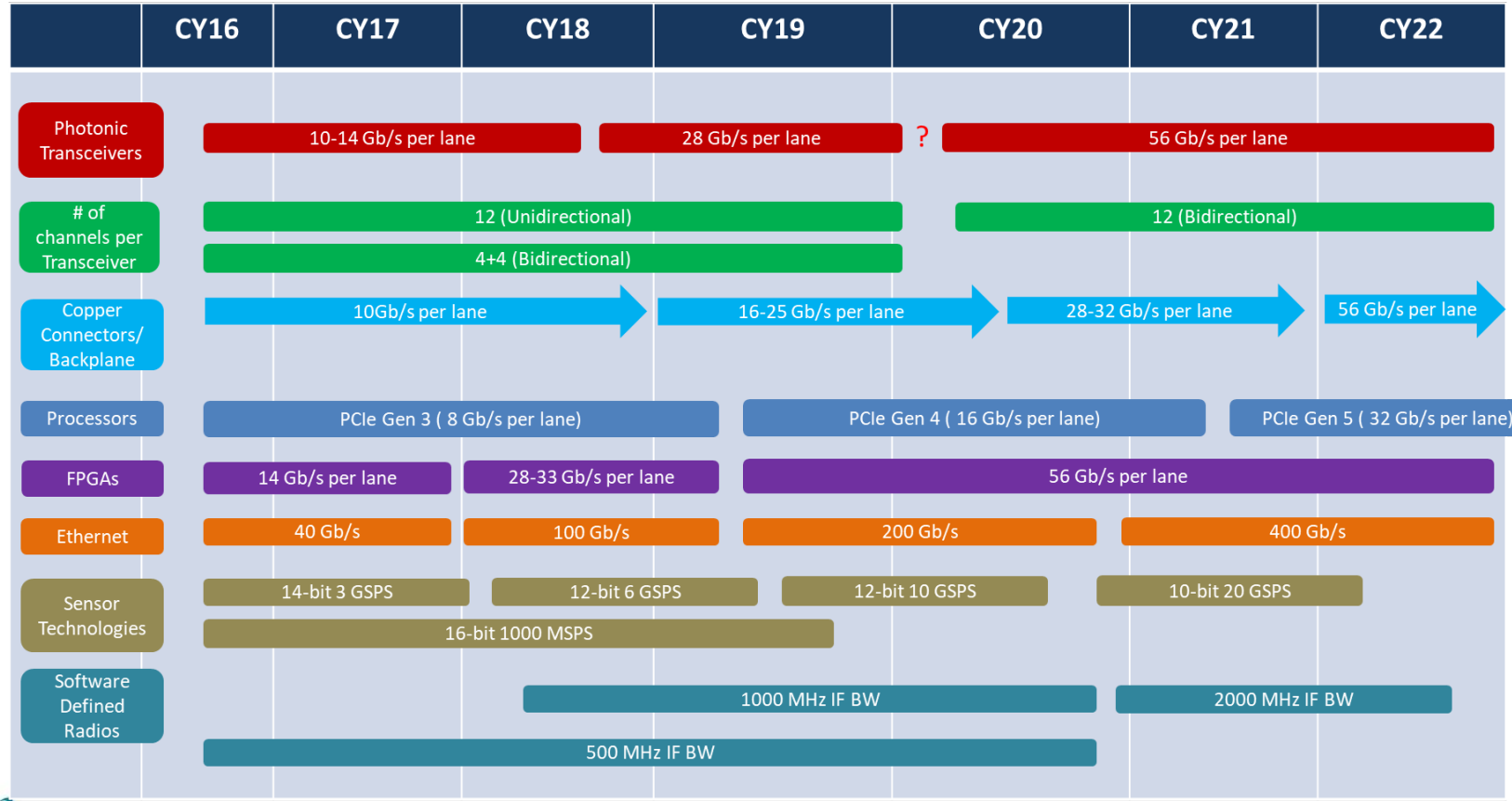
Commercial Hardware Roadmap

SOSA™ Sensor Open Systems Architecture



THE Open GROUP

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Summary

- **HOST is real!**
  - HOST is on contract for ACAT level acquisition programs
- **Tri- service convergence occurring in SOSA**
  - SOSA and CMOSS's collection of standards for OpenRF applications are aligning
  - CMOSS and HOST's collection of hardware are aligning
  - SOSA has become the focal point of embedded system standardization development
- **Tri-service Coordination for a Common Architecture Approach**
  - Establishing a common, tri-service approach to embedded system standardization
  - Using industry standards wherever possible (e.g. VITA, VICTORY, MORA, etc.)
    - Adding specificity where necessary for interchangeability or interoperability
  - Creating / extending standards where necessary
    - Examples include chassis / hardware management

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Georgia Tech Research Institute

Tri-Service Open Architecture Plugfest

Interoperability Demo

HOST/CMOSS/SOSA™ Hardware

January 29, 2020 • Atlanta, GA

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